AMENDMENTS TO THE CLAIMS:

Claims 1-3 (Canceled)

4. (Currently Amended) A semiconductor memory device with a plurality of subblocks each including a drive circuit and a memory array, the device comprising:

a defective line information store circuit for storing information showing defective lines in a plurality of subblocks according to subblocks and

a redundant circuit for substituting other lines including a redundant line for a defective line in each of the plurality of subblocks, ~~on the basis of information stored I the defective line information store circuit~~

wherein the redundant circuit includes a storage circuit for storing the information supplied from the defective line information store circuit, and makes the substitution on the basis of the information stored in the storage circuit.

5. (Original) The semiconductor memory device according to claim 4, wherein the defective line information store circuit is shared by a plurality of subblocks.

6. (Original) The semiconductor memory device according to claim 5, wherein the plurality of subblocks which share the defective line information store circuit are located in the direction perpendicular to the line.

7. (Original) The semiconductor memory device according to claim 5, wherein each of the plurality of subblocks is divided into a plurality of sections, further

wherein the redundant circuit performs a redundant process in each of the plurality of sections.

8. (Original) The semiconductor memory device according to claim 4, wherein the defective line information store circuit is located proximate to a side of one of the plurality of subblocks parallel to the defective line.

9. (Original) The semiconductor memory device according to claim 4, wherein the redundant circuit is located near to one of the plurality of subblocks, the device further comprising:

an address input circuit for receiving an address signal input;

a drive circuit for driving the plurality of subblocks in compliance with the address signal;

a signal line for connecting the address input circuit and the drive circuit; and

a supply circuit for supplying information stored in the defective line information store circuit to the redundant circuit via the signal line.

10. (Original) The semiconductor memory device according to claim 9, wherein the drive circuit is located along a side of one of the plurality of subblocks, further wherein the signal line is located parallel to the drive circuit.